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APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Noh Yeal Kwak

Hyundaijeonjasawan Apt. 109-1401, 441-1
Sadong-Ri, Daewol-Myun, Ichon-Shi
Kyungki-Do, Republic of Korea

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND

1. Field of the Invention

[0001] The invention relates to a method of manufacturing a semiconductor device, and more particularly, to a method of manufacturing a semiconductor device capable of preventing transient enhanced diffusion (TED) phenomenon generated on ions of a well region as well as maintaining activation of ions implanted on the well region to the maximum extent when forming the well area.

2. Discussion of Related Art

[0002] Recently, high-temperature heat treatment processes are used more and more frequently. But, ions implanted into a region forming a device including a semiconductor substrate become diffused during the high-temperature heat treatment process, and therefore characteristics of the device are deteriorated.

[0003] In particular, ions are implanted into an active region for forming a well region before a floating gate of a flash memory device is formed, and the ions for forming a well region must minimize the damage of a semiconductor substrate generated from an ion implantation process performed at high energy and maintain activation ratio of ions implanted into

the well region (that is, coupling strength between ion implanted into a semiconductor substrate and silicon).

[0004] But, the ions formed in a well region so as to satisfy conditions mentioned above become diffused into another film, for example, an oxide film of a element isolation film due to the high-temperature heat treatment process to be performed later and therefore TED phenomenon is brought out.

SUMMARY OF THE INVENTION

[0005] The present invention is contrived to solve the above problems, and the present invention is thus directed to a method of manufacturing a semiconductor device capable of maintaining activation of ions implanted on the well region to the maximum extent when forming the well area, minimizing the damage of a semiconductor substrate when performing an ion implantation process, and preventing transient enhanced diffusion (TED) phenomenon generated on ions of a well region.

[0006] One aspect of the present invention is to provide a method of manufacturing a semiconductor device, comprising the steps of: forming a first well region by performing an ion implantation process for implanting first ions into a semiconductor substrate, and then forming a second well region in the first well region by performing an ion implantation process for implanting second ions having larger mass than the first ions; and forming a well region by performing an annealing process on the result structure.

[0007] In the aforementioned of a method of manufacturing a semiconductor device according to another embodiment of the present

invention, the first well region is formed by implanting phosphorus (P) ions at a tilt angle of 3° to 13° with a dose in the range of 1E11 ions/㎠ to 1E14 ions/㎠ at an energy of about 500 KeV to 3000KeV, by using a high-energy ion implantation device.

[0008] In the aforementioned of a method of manufacturing a semiconductor device according to another embodiment of the present invention, the second well region is formed by implanting arsenic (As) ions having larger mass than phosphorus ions, at a tilt angle of 3° to 13° with a dose of 1E11 ions/㎠ to 1E14 ions/㎠ at an energy of about 100 KeV to 300KeV, by using a middle-current ion implantation device.

[0009] In the aforementioned of a method of manufacturing a semiconductor device according to another embodiment of the present invention, the annealing process is performed using one of an RTP process performed under N_2 or H_2 gas atmosphere at a temperature of 900℃ to 1000℃ for 10seconds to 60 seconds, or a furnace process performed under N_2 or H_2 gas atmosphere at a temperature of 900℃ to 1100℃ for 10minutes to 60 minutes.

[0010] In the aforementioned of a method of manufacturing a semiconductor device according to another embodiment of the present invention, further comprising the steps of forming a region into which ions for adjusting a threshold voltage are implanted on the semiconductor substrate on which well regions are formed, and then forming a tunnel oxide film, a floating gate electrode, a dielectric film and a control gate electrode on an upper part of the semiconductor substrate.

[0011] In the aforementioned of a method of manufacturing a semiconductor device according to another embodiment of the present invention, further comprising a step of forming a screen oxide film serving as a buffer layer for suppressing a damage generated by the ion implantation process for forming the first well region and the second well region before forming the well region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0013] Figs. 1 to 4 are views illustrating a method of forming a well region of a semiconductor device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0014] The present invention will be described in detail by way of following preferred embodiments with reference to accompanying drawings. But, the following preferred embodiments can be modified into other embodiments within the scope of the present invention by those having ordinary skill in the art and access to the teachings of the present invention, and therefore the scope of the present invention is not limited to the following embodiments. In the following explanation, thickness of a layer, etc., in the figures are blown up for convenience and clearness of explanation, and like

reference numerals in the figures are used to identify the same or similar parts. Also, an expression that one layer exists on another layer or on a semiconductor substrate means that one layer may exist on the very another layer or on the semiconductor substrate, or other layer may lie between one layer and another layer or a semiconductor substrate.

[0015] Figs. 1 to 4 are views illustrating a method of forming a well region of a semiconductor device according to a preferred embodiment of the present invention.

[0016] Referring to Fig. 1, a screen oxide film 12 is formed on a front of an upper part of a semiconductor substrate 10. The semiconductor substrate 10 is divided into a region where p-channel transistor is formed (hereafter "PMOS region") and a region where n-channel transistor is formed (hereafter "NMOS region"). A method of forming a well region of the PMOS region is explained specifically in the present invention.

[0017] The screen oxide film 12 is formed for serving as a buffer layer for relieving damage generated in an ion implantation process to be performed later and preventing channeling of ion dopants. At this time, the screen oxide film 12 may be formed in a thickness of 50 to 70Å by means of a wet oxidation method at a temperature of 750 to 800℃.

[0018] Referring to Fig. 2, a first well region 14 is formed by forming a photoresist pattern (PR) on a predetermined region of the result structure and then performing an ion implantation process on the semiconductor substrate 10 using the PR as a mask for implanting ions.

[0019] At this time, the ion implantation process for forming the first well region 14 is performed by implanting phosphorus (P) ions at a tilt angle of 3 to 13° at a dose of 1E11 to 1E14 ions/㎠ at the energy of about 500 to 3000KeV using a high-energy ion implantation device

[0020] Referring to Fig. 3, a second well region 16 is formed by performing an ion implantation process on the first well region 14 using the PR as a mask for implanting ions. At this time, the ion implantation process for forming the second well region 16 is performed by implanting arsenic (As) ions (size 75) having larger mass than phosphorus ions (size 31), which form the first well region 14 , at the tilt angle of 3 to 13° with a dose of 1E11 to 1E14 ions/㎠ at the energy of about 100 to 300KeV using a middle-current ion implantation device. Then, a process of eliminating the PR is performed.

[0021] Referring to Fig. 4, when an annealing process is performed on the front of the result structure, a threefold well region where the second well region 16 is interposed between the first well regions 14 is formed. When an annealing process is performed after the first well region and the second well region are formed, ion density of a source/drain region is increased. Then, the increase of the ion density of a source/drain region makes it possible to prevent TED phenomenon generated due to the high-energy heat treatment process to be performed later such as an oxidation process by decreasing the diffusion speed of the implanted ions. Because ions having large mass and ions having small mass are implanted into same region and mixed, the activation ratio of ions is increased compared with the conventional source/drain region in which only the ions having large mass are implanted.

[0022] Also, it is possible to compensate for the damage of the semiconductor substrate generated in the ion implantation process performed at high energy for forming the first and the second well regions and the damage of the semiconductor substrate generated due to implantation of ions having large mass by performing said annealing process.

[0023] A rapid thermal process (RTP) annealing process or a furnace annealing process may be used as the annealing process mentioned above. The RTP annealing process is performed under N_2 or H_2 gas atmosphere at a temperature of 900 to 1000℃ for 10 to 60 seconds, and the furnace annealing process is performed under N_2 or H_2 gas atmosphere at a temperature of 900 to 1100℃ for 10 to 60 minutes. A screen oxide film 12 is removed after the annealing process.

[0024] A region into which ions for adjusting a threshold voltage are implanted is formed by performing an ion implantation process on the formed well region, and then a tunnel oxide film, a floating gate electrode, a dielectric film and a control gate electrode are formed on the semiconductor substrate on which said region are formed. Then a flash memory device is formed completely.

[0025] According to the embodiment of the present invention, it is possible to prevent TED phenomenon generated due to the high-energy heat treatment process to be performed later such as an oxidation process and to provide the increased activation ratio of ions compared with the conventional source/drain region in which only the ions having large mass are implanted by

performing an annealing process after the first well region and the second well region are formed.

[0026] Also, it is possible to compensate for the damage of the semiconductor substrate generated in the ion implantation process performed at high energy for forming the first and the second well regions and the damage of the semiconductor substrate generated due to implantation of ions having large mass by performing said annealing process.

[0027] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.

[0028] It is therefore intended by the appended claims to cover any and all such changes and modifications within the scope of the present invention.